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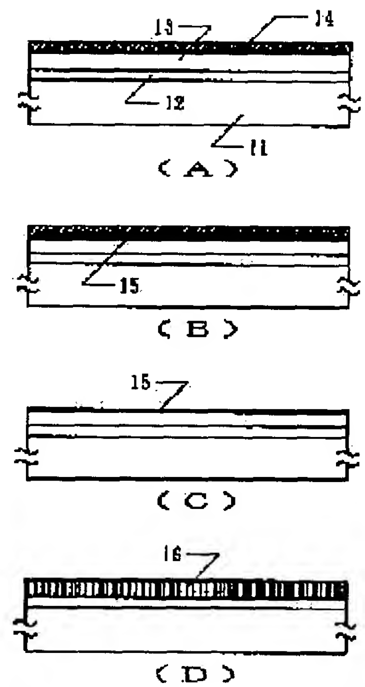
## (54) MANUFACTURE OF SEMICONDUCTOR

(57)Abstract:
PURPOSE: To provide a crystalline silicon film by a method wherein after clusters or the like are formed on a silicon film in the amorphous state, and reacted with amorphous silicon, catalyst material which has not yet reacted is eliminated, and annealing is performed at a temperature lower than the crystallization temperature of ordinary amorphous silicon.
CONSTITUTION: A substratum silicon oxide film 12 of 2000Å in thickness is formed by a plasma CVD method. An amorphous silicon film 13 is deposited to be 1500Å thick by a plasma CVD method, and a nickel film 14 is deposited by a sputtering method. After that, the nickel film is made to react with the amorphous silicon film 13, and a thin crystalline silicon layer 15 is formed on the interface. Then annealing is performed for 8 hours in a nitrogen atmosphere at 450-580°C in an annealing furnace. By the above process, the amorphous silicon film is crystallized, and a crystalline silicon film 16 can be obtaied.




LEGAL STATUS

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CLAIMS

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[Claim(s)]
[Claim 1] The 1st process which forms the silicon layer of the amorphous status substantially on a substrate, The 2nd process which forms nickel, iron, cobalt, and the catalyst material containing at least one of platinum on the aforementioned silicon layer, The 3rd process to which the front face and catalyst material of the aforementioned amorphous silicon are made to react, The manufacture technique of the semiconductor characterized by having the 4th process which removes a catalyst material after the aforementioned process, and the 5th process which anneals a substrate at temperature lower than the crystallization temperature of an amorphous silicon after the aforementioned process.
[Claim 2] It is the manufacture technique of the semiconductor which the catalyst material used at the 2nd process contains silicon and nickel in a claim 1, and is characterized by the composition ratio being silicon / nickel =0.4-2.5.
[Claim 3] It is the manufacture technique of the semiconductor characterized by the annealing temperature of the 5th process being lower than the crystallization temperature of a usual amorphous silicon 20-150 degrees C in a claim 1.
[Claim 4] It is the manufacture technique of the semiconductor characterized by performing the 4th process in a claim 2 using a hydrochloric acid or fluoric acid.

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[Translation done.]

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to the technique of obtaining the crystalline semiconductor used for thin film devices, such as a thin film-like insulated gate field effect transistor (TFT or TFT).
[0002]
[Description of the Prior Art] Conventionally, the crystalline silicon semiconductor thin film used for thin film devices, such as a thin film-like insulated gate field effect transistor (TFT), crystallizes the amorphous silicon layer formed by the plasma CVD method or heat CVD on insulating front faces, such as an insulating substrate, over the long time of 12 hours or more at the temperature of 600 degrees C or more in the equipment of an electric furnace etc., and was produced. It was asked for more nearly prolonged heat treatment in order to acquire sufficient property (the high electrolysis effect mobility and high reliability) especially.
[0003]
[The technical probrem which invention will solve and to carry out] However, such conventional technique was holding many technical probrems. A throughput of one is low, therefore it is that a cost becomes high. For example, when this crystallization process should take 24 hours, 2 minutes, then 720 substrates had to be simultaneously processed for the processing time per substrate. however, for example, by the tubular furnace usually used, as for the number of sheets of the substrate which can be processed at a time, when 50 sheets come out at most and use only one equipment (coil), time has taken no less than 30 minutes per sheet That is, in order to have made the processing time per sheet into 2 minutes, 15 had to use the coil. It meant that an investment scale expands this and a depreciation of the investment being large and rebounding upon the cost of a product.
[0004] Another problem was the temperature of heat treatment. Usually, the substrate used for production of TFT is divided roughly into the boro-silicated glass of what consists of pure oxidization silicon like quartz glass, and the non-alkali like Corning, Inc. of No. 7059 (henceforth Corning 7059). Among these, the former is excellent in thermal resistance, and since the same handling as the wafer process of a usual semiconductor integrated circuit can be performed, about temperature, it is satisfactory [ the former ] in any way. However, the cost is high and increases abruptly exponentially with the increase in substrate area. Therefore, now, it is comparatively used only for TFT integrated circuit of a facet product.
[0005] On the other hand, although the cost was fully low when the alkali free glass was compared with the quartz, there is a problem in respect of thermal resistance, and generally it was distorted, and since the point was 600 degrees C or less with about 550-650 degrees C, especially the material which is easy to come to hand, by 600-degree C heat treatment, the problem of irreversible deflation and an irreversible camber arose in the substrate. In a big thing by which especially a substrate exceeds 10 inches of vertical angles, it was remarkable. Since it was above, about crystallization of a silicon semiconductor layer, 550 degrees C or less and the heat treatment conditions of less than 4 hours were made indispensable to cost reduction. this invention aims at offering the production technique of the semiconductor which clears such conditions, and the production technique of the semiconductor device using such a semiconductor.
[0006]
[Means for Solving the Problem] this invention The amorphous status or the disorderly crystallized state which can be substantially called amorphous status On the silicon layer in (for example, the status that the crystalline good fraction and the amorphous fraction are intermingled), nickel, Iron, cobalt, the layer containing at least one of platinum, grain, a cluster, etc. After having formed (it is hereafter called a catalyst material) and making this react with an amorphous silicon first, An unreacted catalyst material is removed and it is characterized by obtaining a crystalline silicon layer by annealing at temperature lower subsequently than the crystallization temperature of a usual amorphous silicon, and desirable temperature low 20-150 degrees C, for example, the temperature of 580 degrees C or less.
[0007] This invention people considered reducing the obstruction energy of the aforementioned process by a certain catalysis completely apart from the idea of the conventional solid phase crystallization. It was easy to combine nickel (nickel), iron (Fe), cobalt (Co), and platinum (Pt) with silicon, for example, this invention people became silicification nickel (chemical formula $NiSi_x$ and $0.4<=x<=2.5$) easily, when it was nickel, and they directed their attention to the lattice constant of silicification nickel being close to the thing of a silicon crystal. Then, it became clear that an amorphous silicon reacts easily by the interface with silicification nickel, and a reaction called amorphous silicon + silicification nickel -> silicification nickel

+ crystal silicon arises as a result of carrying out the simulation of the energy of a 3 yuan system of a crystal silicon-silicification nickel-amorphous silicon etc. The potential barrier of this reaction is fully low, and is low. [ of the temperature of a reaction ]

[0008] As for this reaction formula, the nickel atom shows building an amorphous silicon to crystal silicon and changing. In fact, it was 580 degrees C or less, and a reaction is started and it became clear that at least 450 degrees C of reactions are observed. Moreover, the crystal silicon obtained by this reaction had good crystallinity. However, the nickel atom itself is not desirable for the silicon as a semiconductor material. Then, the process which removes a nickel atom is required. What is necessary is just to use a hydrochloric acid (HCl) or fluoric acid (HF) for this. Although these acids erode nickel and silicification nickel, an amorphous silicon and crystal silicon do not invade.

[0009] If the crystal silicon formed of the above-mentioned reaction remains even if it removes a nickel atom, it can crystallize by making this into a nucleus. It became clear that it makes this a nucleus since the crystallinity of the silicon crystal generated by the above-mentioned reaction as above-mentioned is good, and crystallization of an amorphous silicon is promoted. Typically, it was shown that it can crystallize at temperature low 20-150 degrees C as compared with the crystallization temperature of a usual amorphous silicon. Moreover, the time which a crystal growth takes was also shortened conventionally. Although it is natural, the speed at which crystallization advances is so quick that temperature is high. Moreover, the same reaction was seen although iron, cobalt, and platinum were also inferior to nickel.

[0010] It is desirable to use the layer containing nickel, iron, cobalt, a platinum simple substance, or its silicide, grain, a cluster, etc. as a catalyst material in this invention. However, an oxide is not desirable in the above-mentioned element. An oxide is a stable compound and this is because the above-mentioned reaction cannot be started.

[0011] Moreover, the orientation of a crystal growth is controllable by especially this invention by preparing the above-mentioned catalyst material alternatively. The crystal silicon obtained using such technique is convenient, in using for semiconductor devices, such as TFT, since it has the structure near the single crystal with a crystalline sufficient continuity over long distance unlike the conventional solid phase epitaxial growth.

[0012] Moreover, such a result (crystallization speed) with the good amorphous silicon layer as a start material of this crystallization was obtained that there is little hydrogen concentration. However, since hydrogen was emitted according to advance of crystallization, the so clear correlation was not regarded for the hydrogen concentration in the obtained silicon layer as the hydrogen concentration of the amorphous silicon layer of a start material. The hydrogen concentration in the crystal silicon by this invention was below pentatomic % more than 0.01 atom % typically. Furthermore, in order to acquire good crystallinity, in an amorphous silicon layer, it is so good that there is little concentration of carbon, nitrogen, and oxygen, and to be three or less [ 1x1019cm - ] is desired.

[0013]

[Example] [Example 1] The nickel layer on Corning 7059 glass substrate is formed, an amorphous silicon layer is crystallized, using this as a catalyst, and how to obtain a crystal silicon layer is explained on the basis of drawing 1 . On the substrate 11, the substratum oxidization silicon layer 12 of thickness 2000** was formed by the plasma CVD method. next, a plasma CVD method -- the amorphous silicon layer 13 -- 500-3000** -- for example, 1500** deposition of was done and hydrogen **** was performed among the nitrogen ambient atmosphere 430 degrees C, 0.1 - 2 hours (for example, 0.5 hours) then, a spatter -- the nickel layer 14 -- thickness 100-1000** -- for example, 500** deposition of was done The good result was obtained when 100-500 degrees C of substrates were preferably heated at 180-250 degrees C at the time of membrane formation of nickel. This is for adhesion of the layer [ the silicon layer and nickel layer ] of a substratum to improve. Silicification nickel could be used instead of nickel. ( Drawing 1 (A))

[0014] Then, heated at 450-580 degrees C only for 1 to 10 minutes, the above-mentioned nickel layer 14 and the amorphous silicon layer 13 were made to react, and the thin crystal silicon layer 15 was formed in the interface. Although this crystal silicon layer thickness depended at reaction temperature and time, on the conditions for 550 degrees C and 10 minutes, it was about 300**. ( Drawing 1 (B))

[0015] Next, it reacted with the nickel layer and the nickel layer, and the produced silicification nickel layer was etched with 5 - 30% of the hydrochloric acid. At this etching, there was no influence in the crystal silicon produced by the reaction of an amorphous silicon and nickel (silicification). ( Drawing 1 (C))

Subsequently, this was annealed in the 8 hour nitrogen ambient atmosphere among annealing kiln at 450-580 degrees C, for example, 550 degrees C. According to this process, the amorphous silicon layer was able to be crystallized and the crystal silicon layer 16 was able to be obtained. Raman scattering of the crystal silicon obtained at this time -- the result of a spectrum and X-ray diffraction is shown in drawing 3 and the drawing 4 In drawing 3 , C-Si is the Raman spectrum of the single crystal silicon which is a standard sample. Moreover, the Raman spectrum from which (a) was obtained by this example, and (b) are the Raman spectrums when annealing the usual amorphous silicon which does not have a catalyst material on condition that the above. It turns out that good crystal silicon was obtained by this invention.

[0016] [Example 2] this example is shown in drawing 2 . The substratum oxidization silicon layer 22 of thickness 2000** was formed by the plasma CVD method on the Corning 7059 glass substrate 21. next, a plasma CVD method -- the amorphous silicon layer 23 -- 500-3000**, for example, 500**, -- and 1500** deposition of was done and hydrogen **** was performed among the nitrogen ambient atmosphere 430 degrees C, 0.1 - 2 hours (for example, 0.5 hours)

[0017] then, a spatter -- a nickel layer -- thickness 100-1000** -- for example, 500** deposition of was done Silicification nickel could be used instead of nickel. Thus, the patterns 24a, 24b, and 24c which etch and show the formed nickel layer in

drawing were formed. ( Drawing 2 (A))
Then, heated at 450-580 degrees C only for 1 to 10 minutes, the above-mentioned nickel layers 24a-24c and the amorphous silicon layer 23 were made to react, and the thin crystal silicon fields 25a, 25b, and 25c were formed in the interface. ( Drawing 2 (B))
[0018] Next, it reacted with the nickel layer and the nickel layer, and the produced silicification nickel layer was etched with 5 - 30% of the hydrochloric acid. At this etching, there was no influence in the crystal silicon 25a-25c produced by the reaction of an amorphous silicon and nickel (silicification). ( Drawing 2 (C))
Next, this was annealed in the 4 hour nitrogen ambient atmosphere among annealing kiln at 450-580 degrees C, for example, 550 degrees C. Drawing 2 (D) is the intermediate state, and crystallization advances from the crystal silicon fields 25a-25b formed previously, and it shows a mode that the crystal silicon fields 26a, 26b, and 26c are expanded all over the amorphous field 23.
[0019] Finally all amorphous silicon layers were crystallized and the crystal silicon layer 27 was obtained. By this example, it goes on from a nickel pattern in longitudinal direction to going on perpendicularly like [ the orientation of a crystal growth / front face ] a substrate side in the example 1. For example, the crystal silicon fields 26a-26c shown in drawing 2 (D) have the structure respectively near a single crystal. For this reason, it is comparatively rare for potential barriers, such as a grain boundary, to arise in longitudinal direction, and it is convenient in using for TFT etc. It is not desirable to use the fraction in the fraction with which it corrects, for example, the crystal silicon fields 26a and 26b collide, since the defect of a crystal is large. The result which measured the crystallization speed by this example is shown in drawing 5 . It became clear that crystallization advances so quickly that a silicon layer is thick.
[0020]
[Effect of the Invention] As mentioned above, as stated, it is epoch-making in the meaning that this invention promotes low-temperature-izing of amorphous silicon crystallization, and short-time-ization, the facility for it, equipment, and technique are very common, and the profits brought to industry since it excels in mass-production nature plan, and it cannot carry out.
[0021] For example, in the conventional solid phase grown method, since annealing of at least 24 hours was needed, although, as for 2 minutes, then annealing kiln, the substrate processing time per sheet was needed also for 15, since it was shortened within 4 hours, the number of annealing kiln is reducible [ with this invention ] to 1/6 or less. The enhancement in the productivity by this and curtailment of the amount of capital investment lead to a fall of a substrate processing cost, as a result lead to a fall of TFT price, and evocation of the new need by it. Thus, this invention is suitable for it being useful and being patented on industry.

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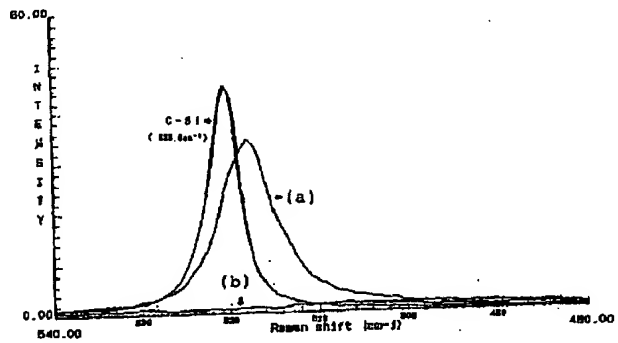
* NOTICES *

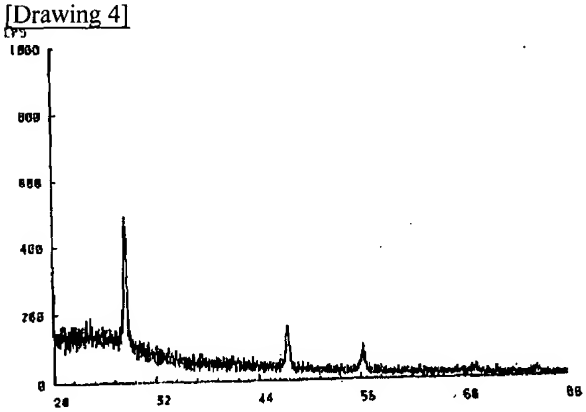


DRAWINGS

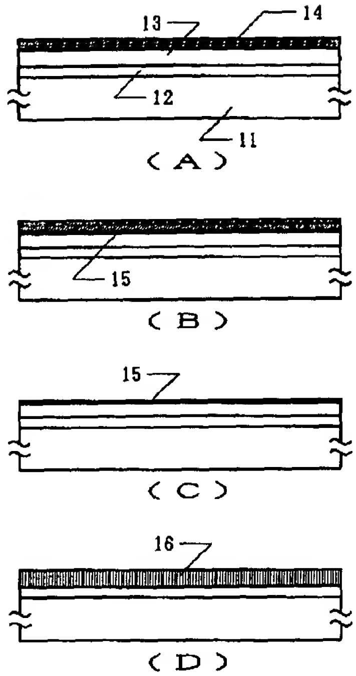
[Drawing 3]



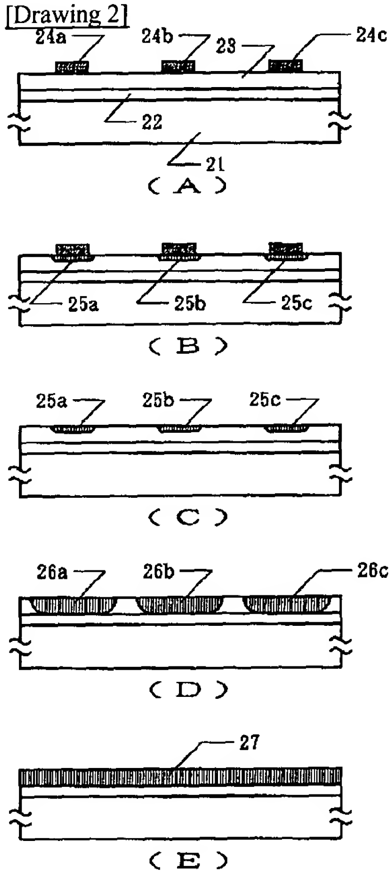

[Drawing 4]



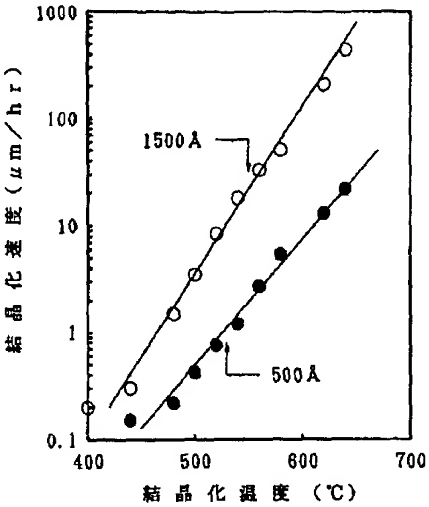
[Drawing 1]




[Drawing 2]




[Drawing 5]

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